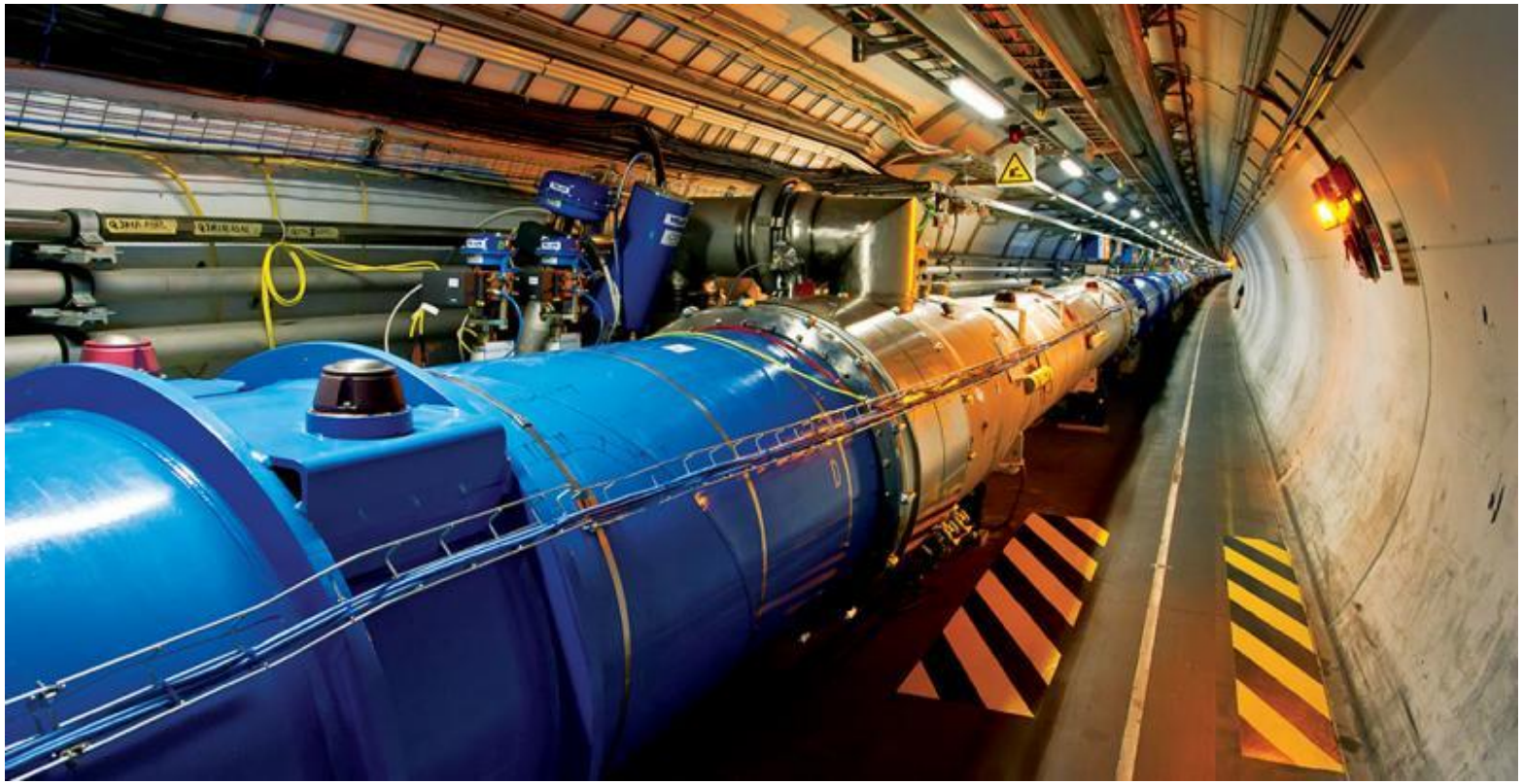


High DR ADC for LHC

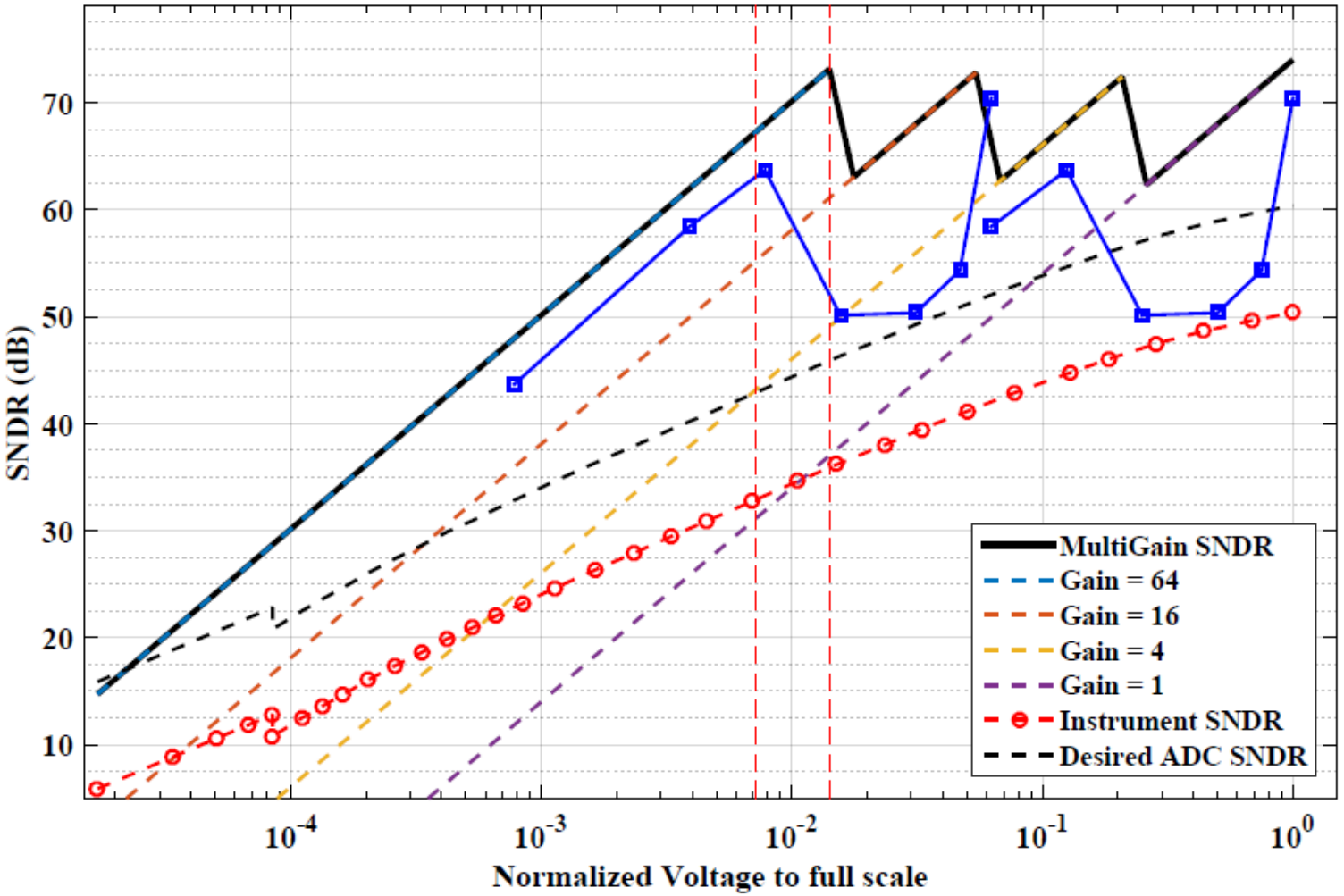
Sarthak Kalani

Last updated: 03/31/17

COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

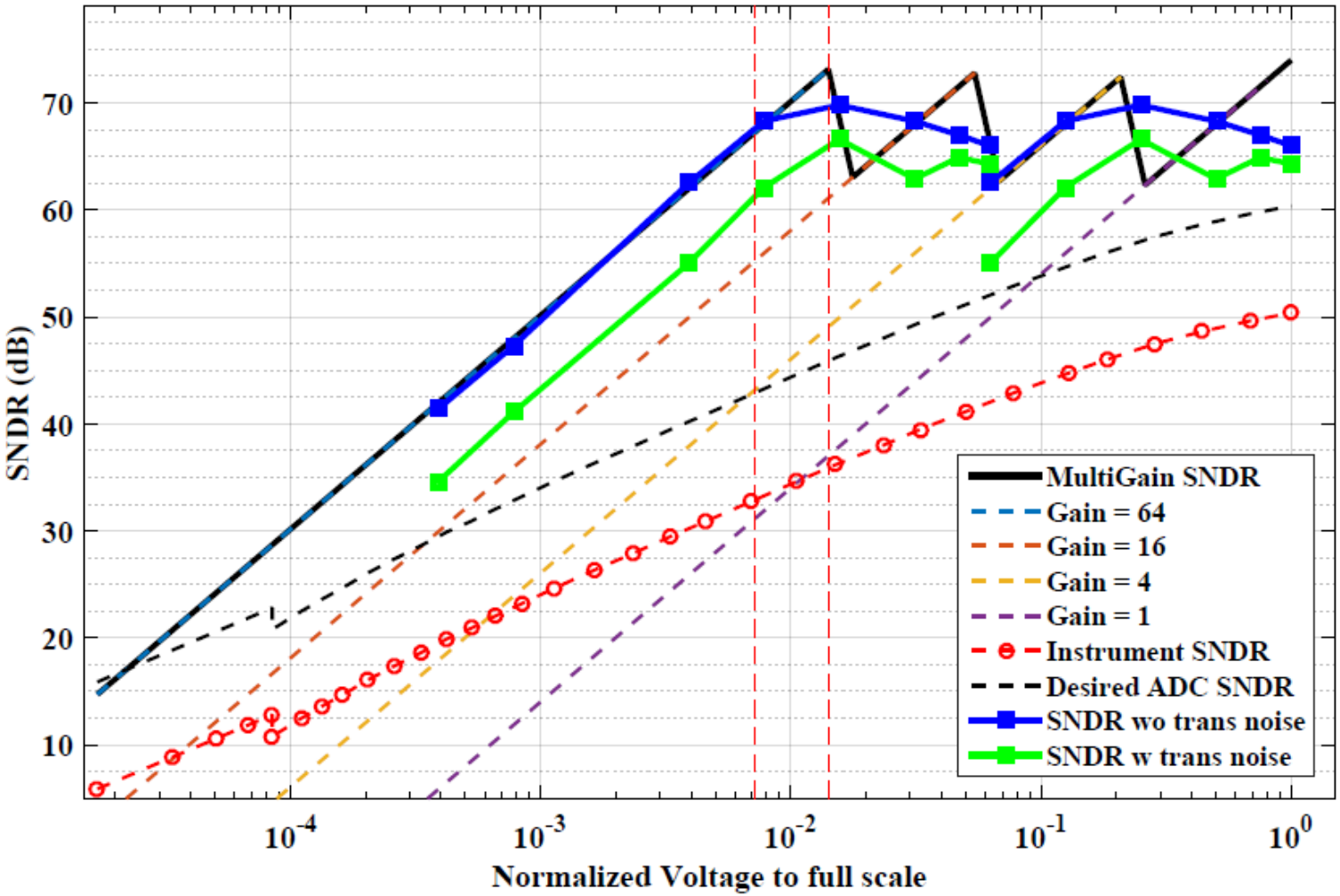
Columbia Integrated Systems Laboratory

Previously, with autoselect:



- Auto select means verilogA logic block determines whether to choose 1x gain or 4x gain, based on input.

Current status, with autoselect:



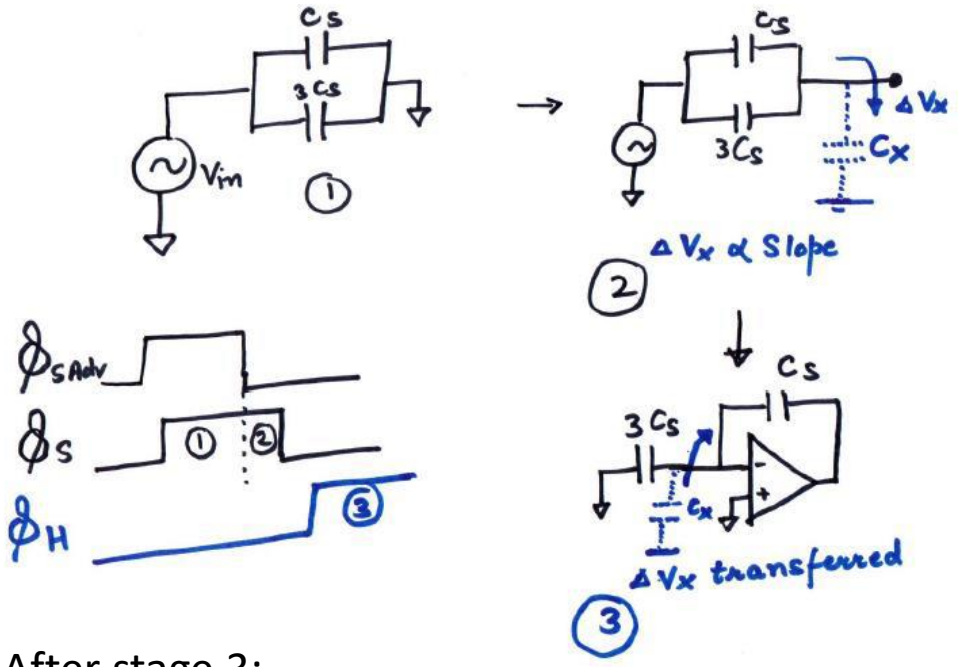
Simulations include:

- Bond wire: 4nH
- Load cap: 4pF
- Transistor level transient noise
- Real Caps

- Auto select means verilogA logic block determines whether to choose 1x gain or 4x gain, based on input.

Why autoselect was not working?

- Parasitic Cap at virtual ground node gets charged and affects output by the same amount (irrespective of gain)
- When samples are combined, if 1x samples are offset by k_{1x}, then 4x samples are offset by $k_{1x}/4$
- This limits max SNDR achieved



After stage 3:

$$V_{OUT} = Asin(\omega t) + k.C_X.A.\omega.cos(\omega t).\Delta t$$

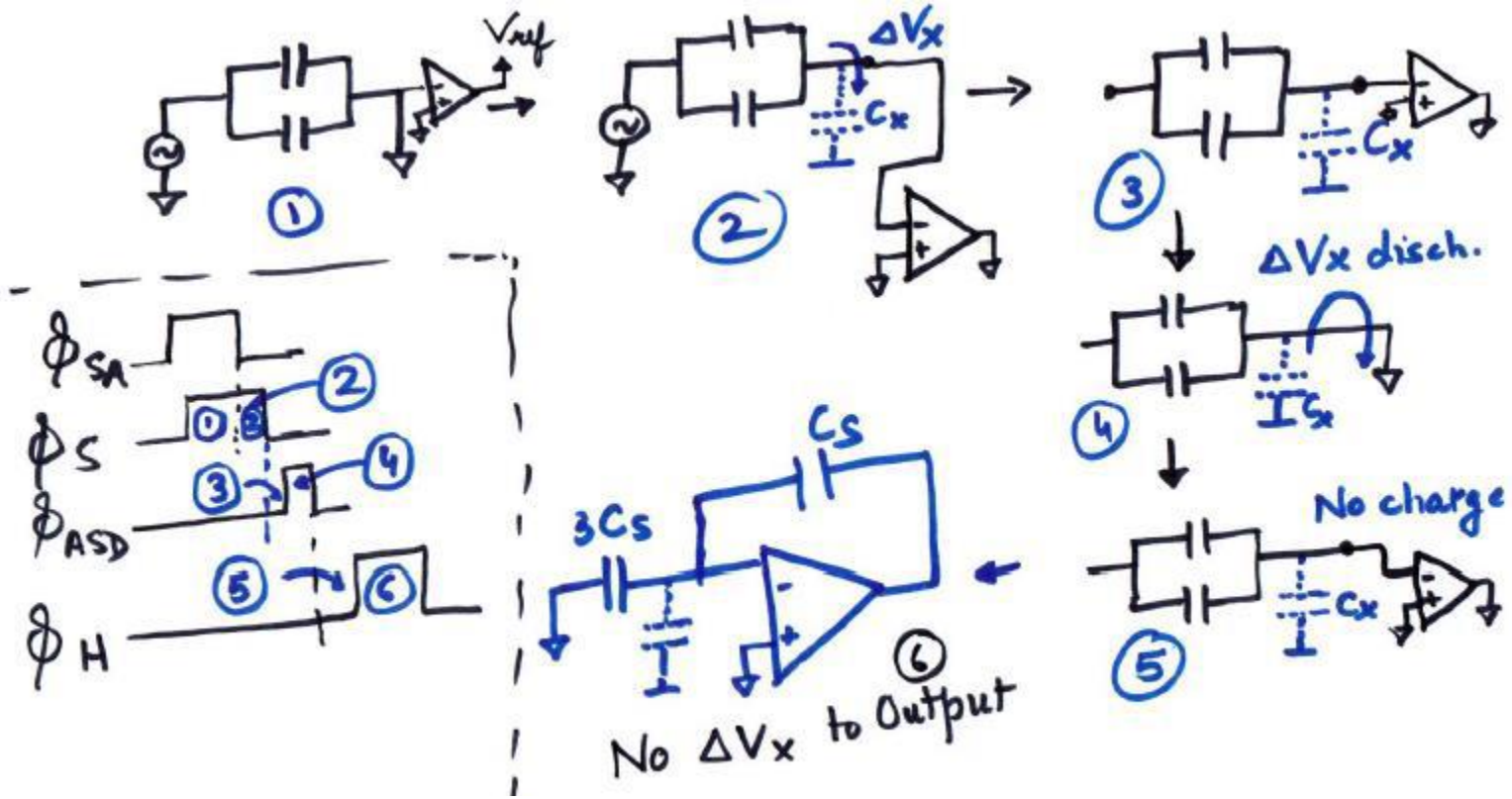
for gain of 1x &

$$V_{OUT} = 4Asin(\omega t) + k.C_X.A.\omega.cos(\omega t).\Delta t$$

for gain of 4x

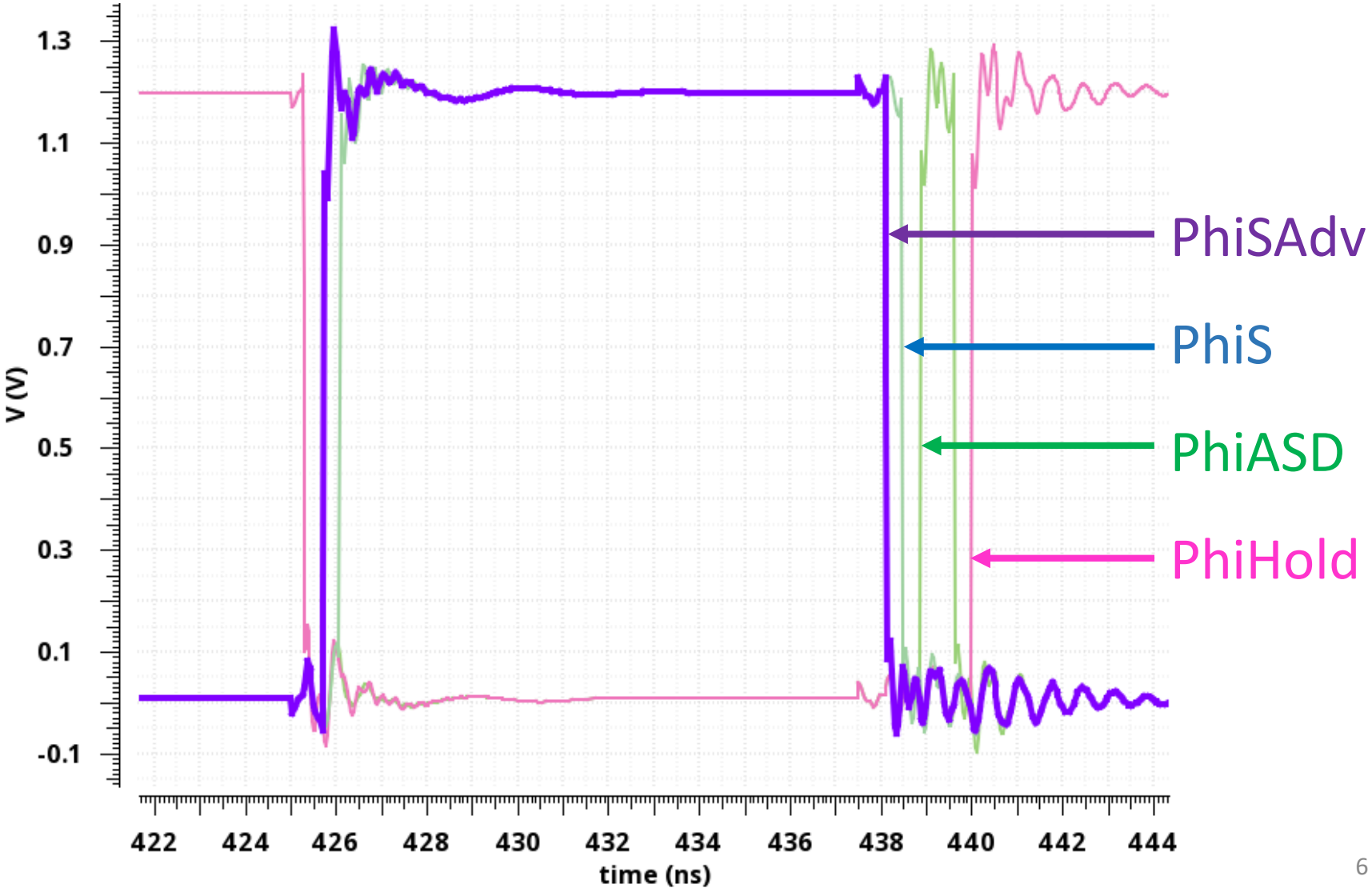
Proposed solution: Introduce ASD clock

- Autozero slope distortion (ASD) clock discharges C_X before hold clock starts.

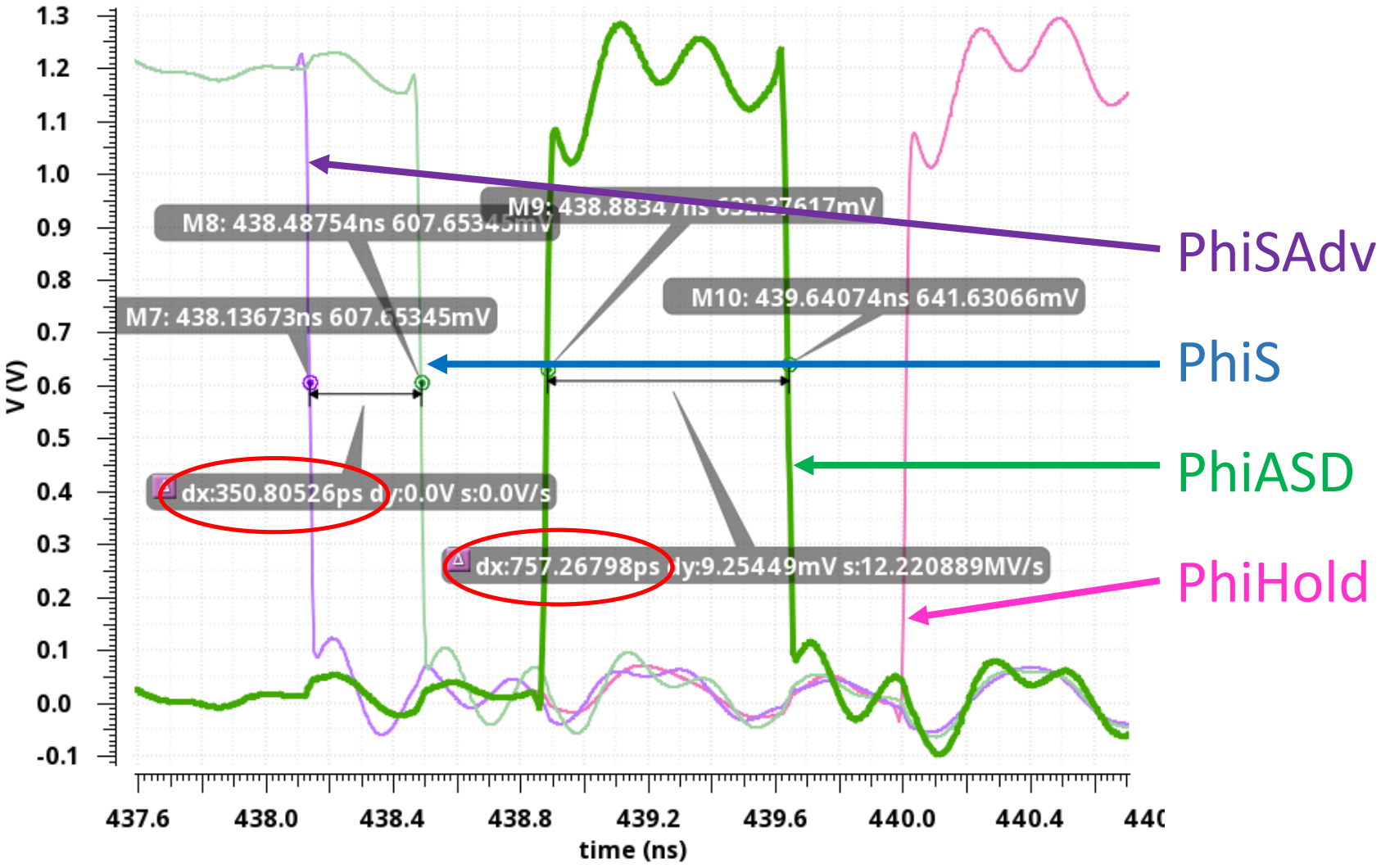


Result: Good SNDR for autoselect!

Clock waveforms



Clock waveforms

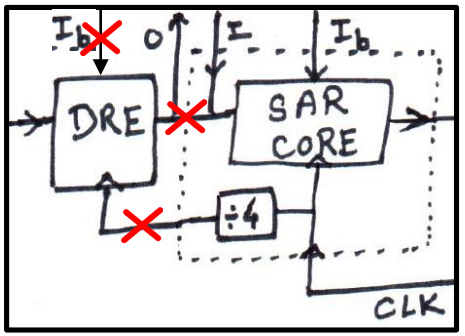


Enough non overlap margins available

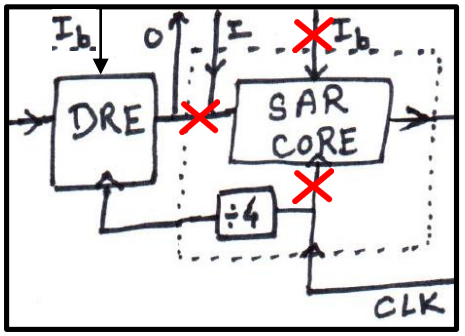
Test Strategy

- SAR only:
  - DRE clock disabled
  - DRE bias disabled
  - SAR input from outside
  - Exact power number not needed
- DRE only:
  - ADC clock disabled
  - ADC bias disabled
  - DRE output taken out
  - SAR power, negligible if SAR clock is disabled
- Both SAR and DRE:
  - The clocks to both the blocks enabled
  - Middle pins disabled
  - DRE output -> SAR -> Serializer

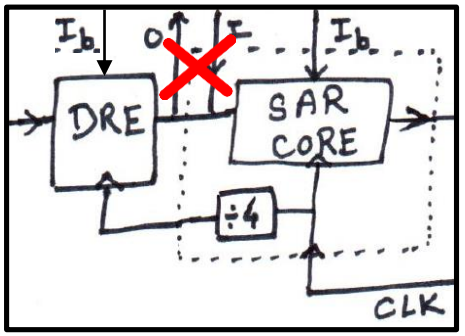
SAR Test



DRE Test



DRE and SAR Test



Next steps and Timeline

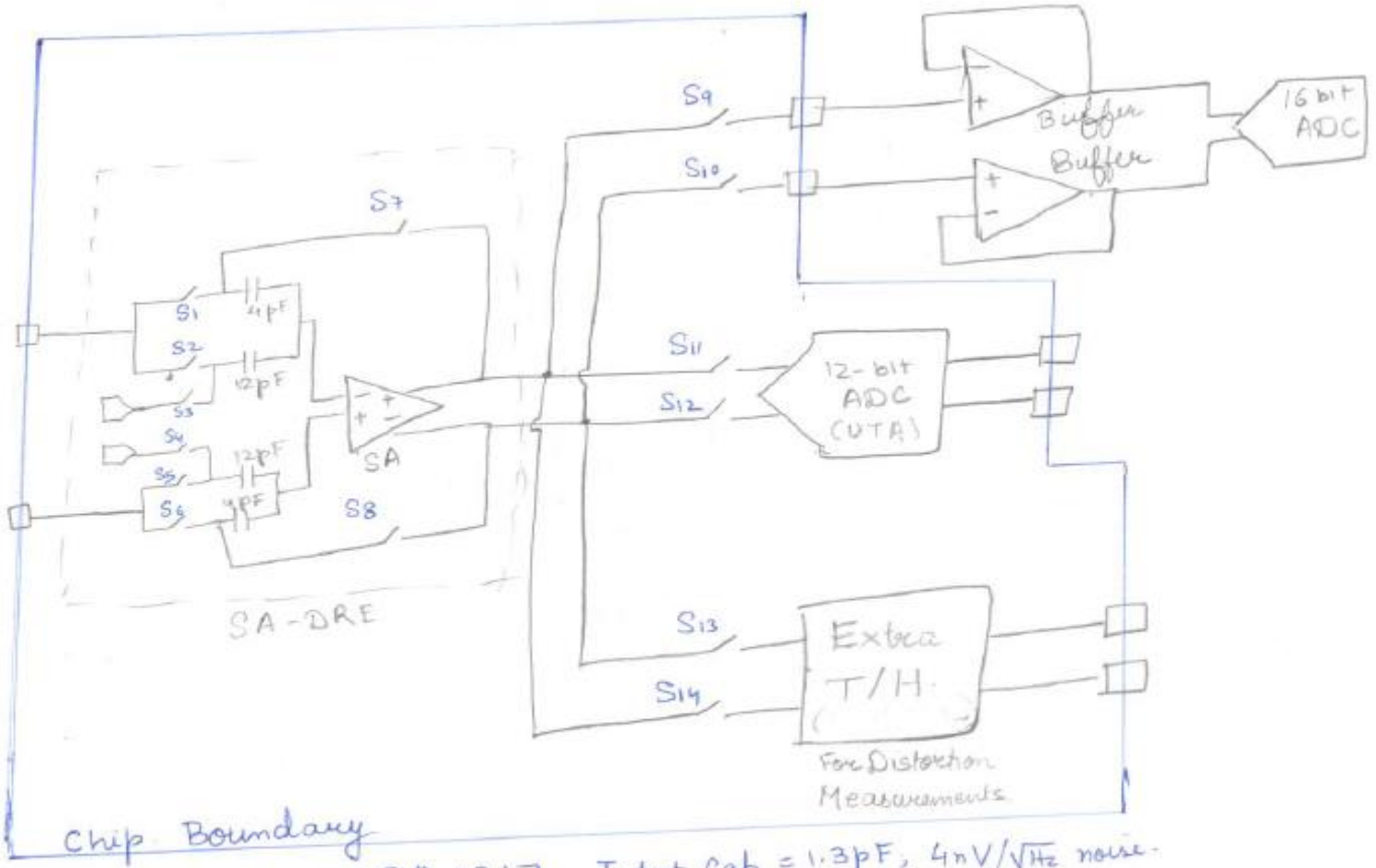
- Start layout
- Integrate scan chain
- Connect with 12-bit ADC.

- If time permits:
  - Low frequency T&H
  - Implement calibration scheme in Matlab

S.No.	Item	Complete by
1	Layout of individual blocks	Apr 5th, 2017
2	Top level routing, pad connections	Apr 13th, 2017
3	Integration with SAR-ADC	Apr 20th, 2017
4	PEX, functionality test	Apr 23rd, 2017

Backup Slides

PCB level schematic



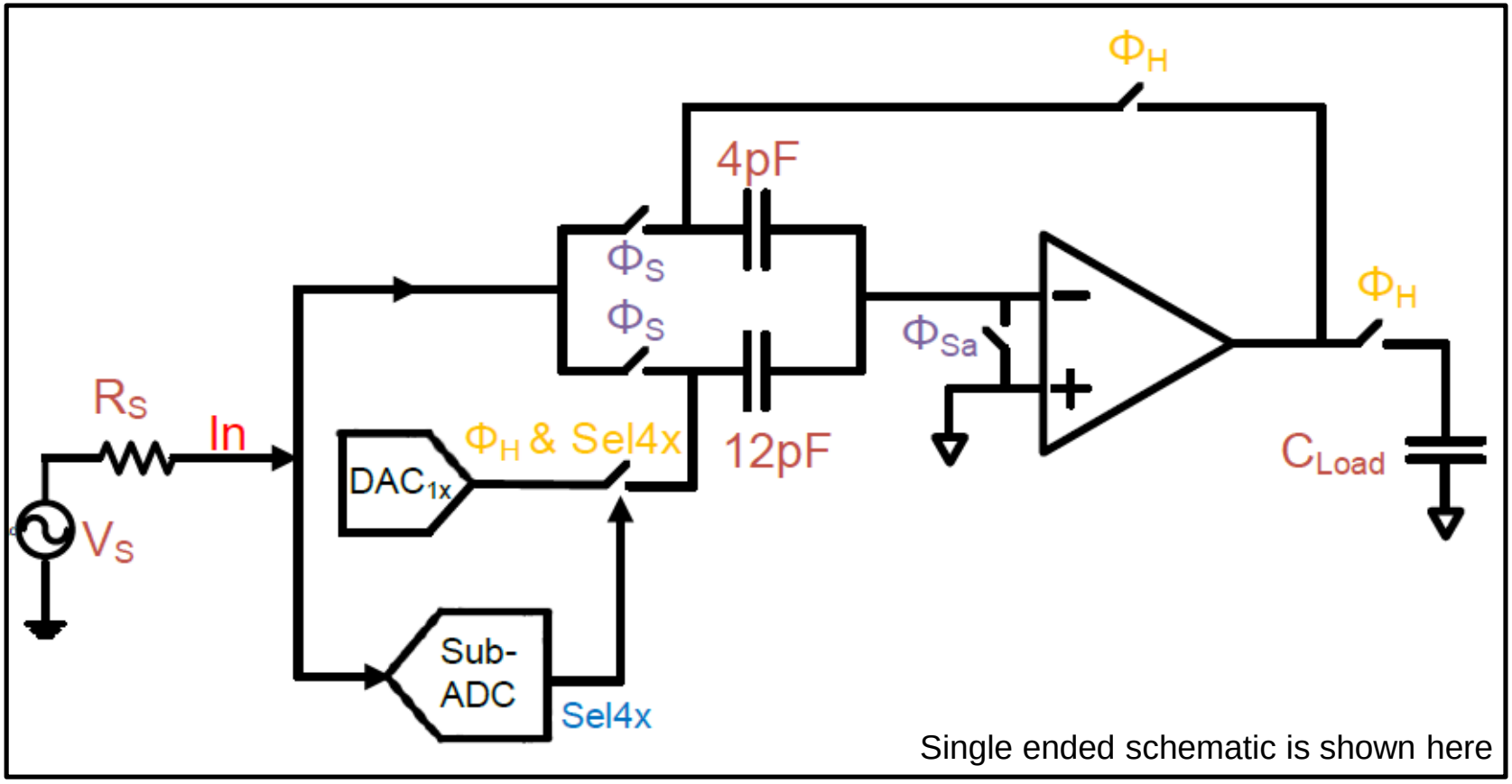
External Buffer = ADA 4817, Input Cap = 1.3pF, 4nV/√Hz noise.

External ADC = AD 9650, 1.8V supply, 2.7Vpp output,

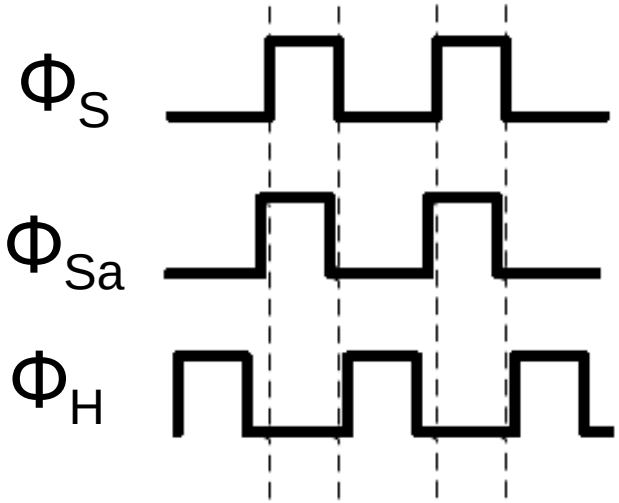
83 dB SNDR, 25MSPS to 105MSPS

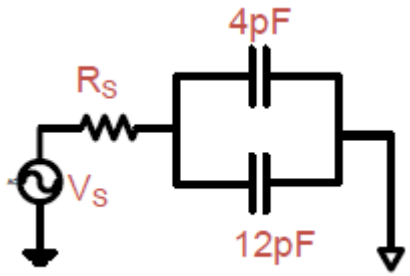
Sampling Amplifier (SA) based DRE

Small input: 4x gain Large input: 1x gain

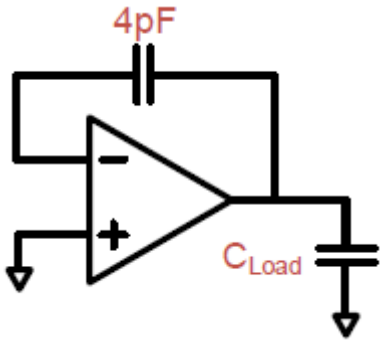


SA-DRE timing diagram

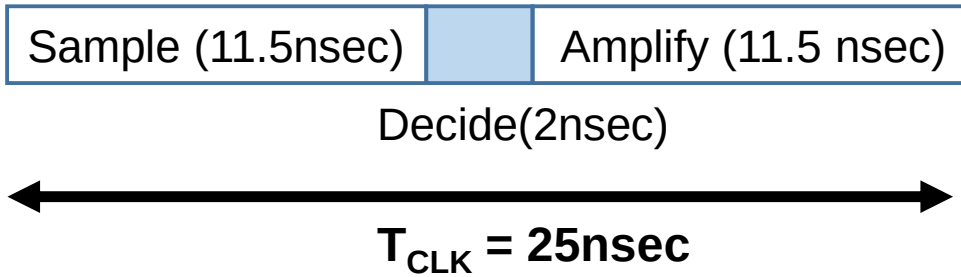


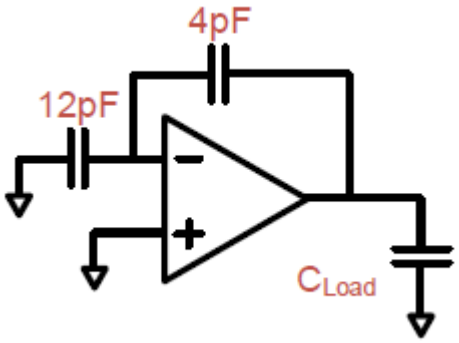


Sample Phase



Hold Phase & 1x Selected





Hold Phase & 4x Selected

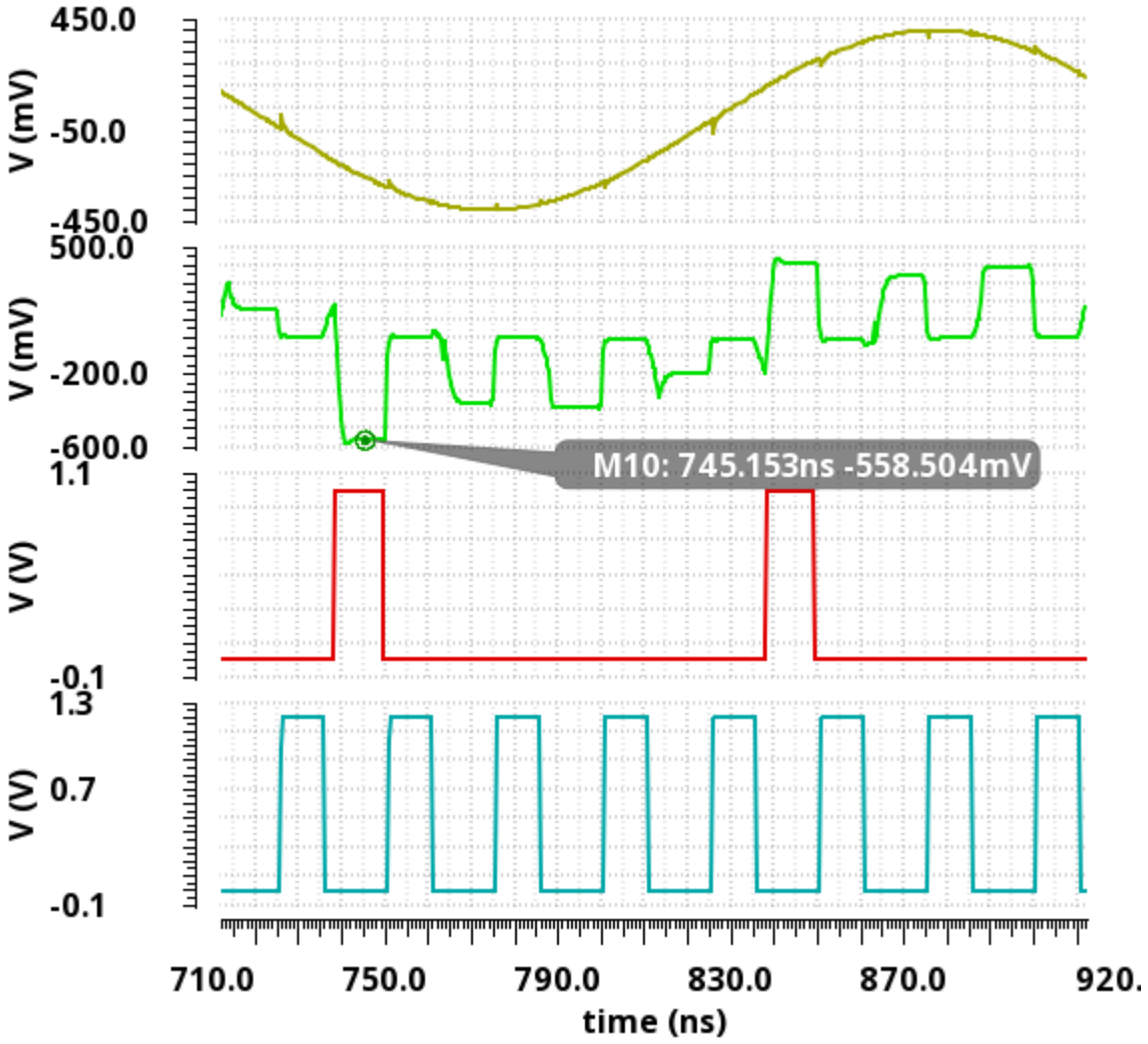
Auto select timing diagram

Differential Input

Differential Output

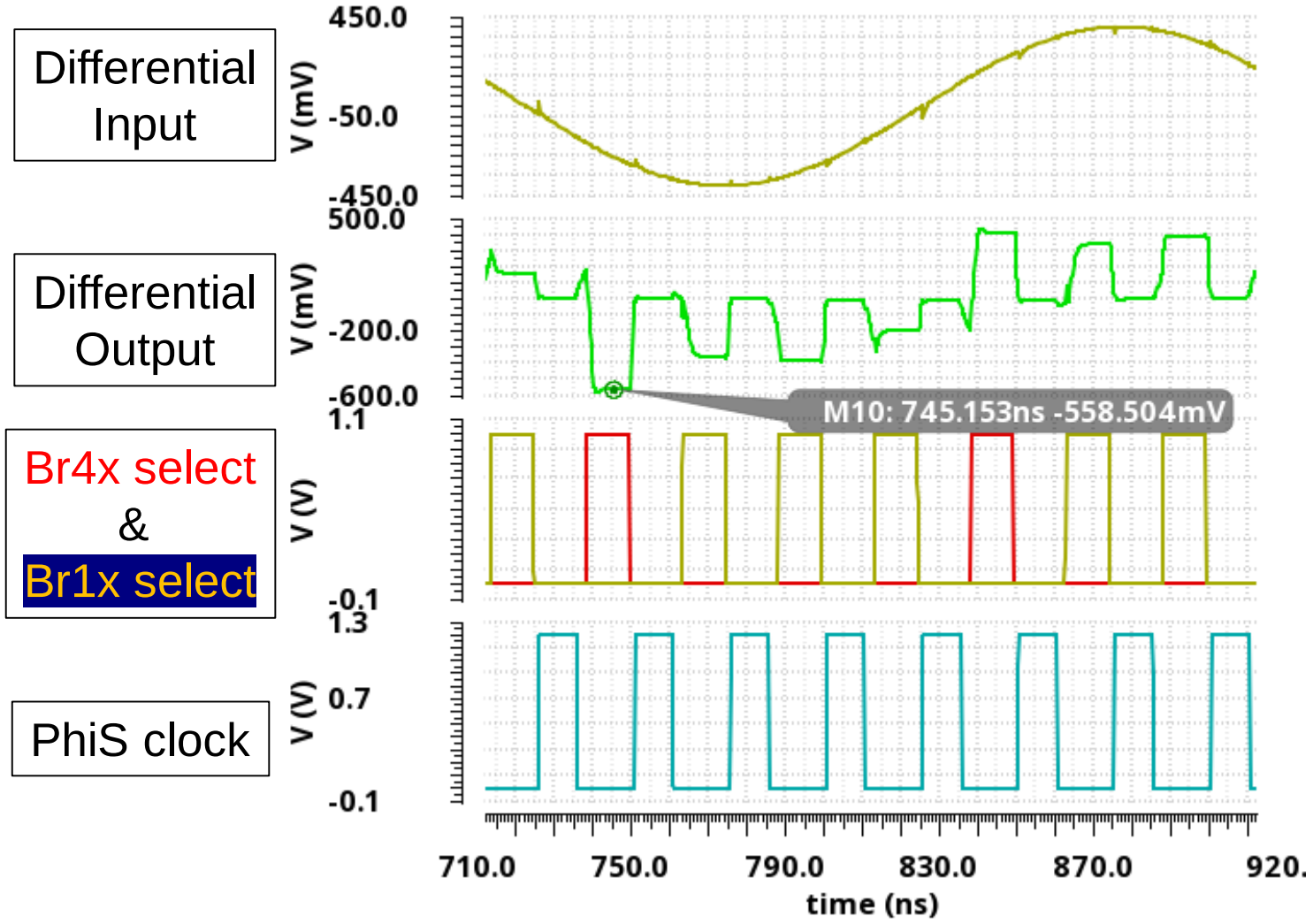
Br4x select

PhiS clock



- Vin = 400mV,
- Autoselect enabled

Auto select timing diagram



- Vin = 400mV,
- Autoselect enabled

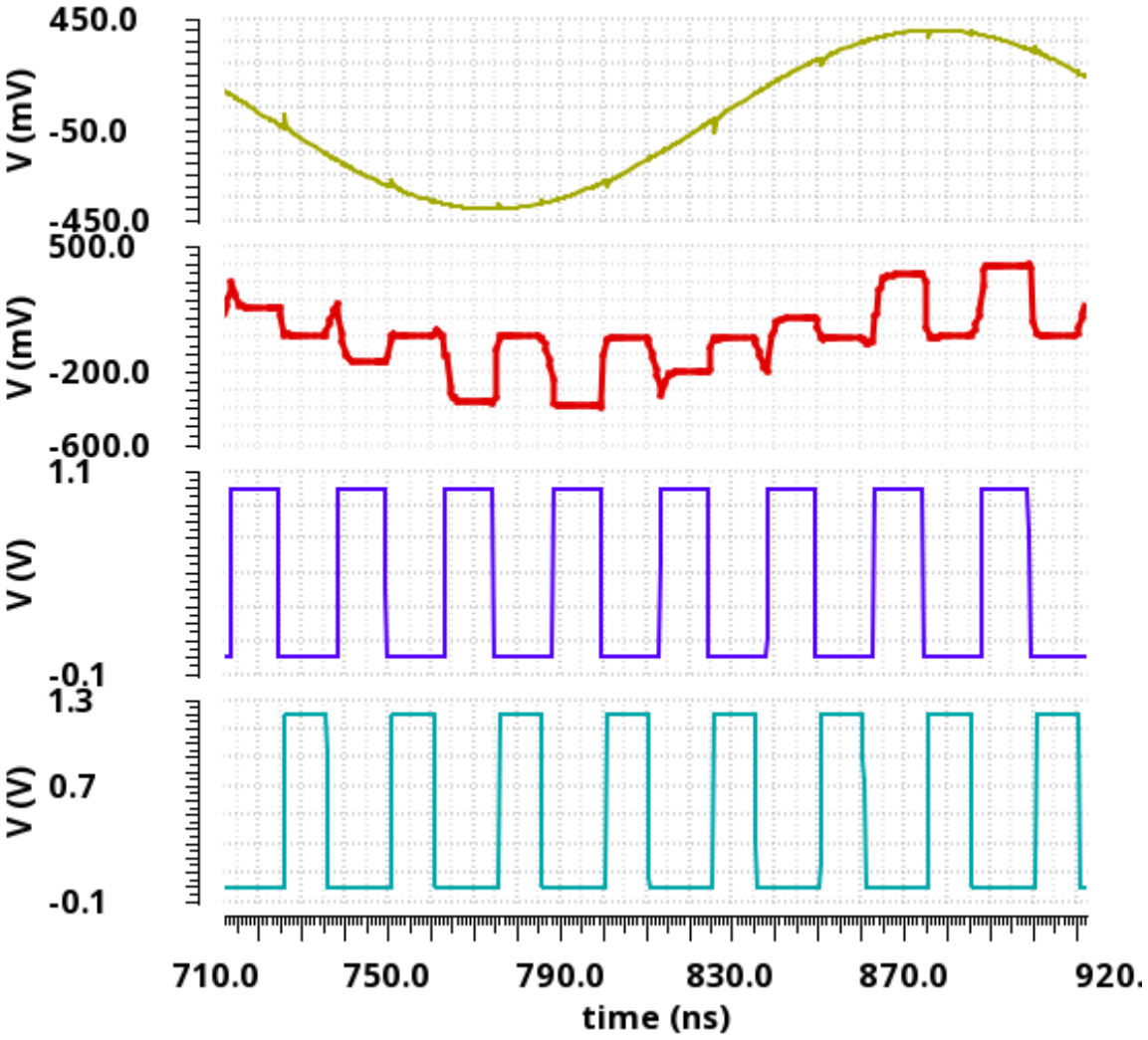
Manual select timing diagram

Differential Input

Differential Output

Br1x Select
Always enabled

PhiS clock



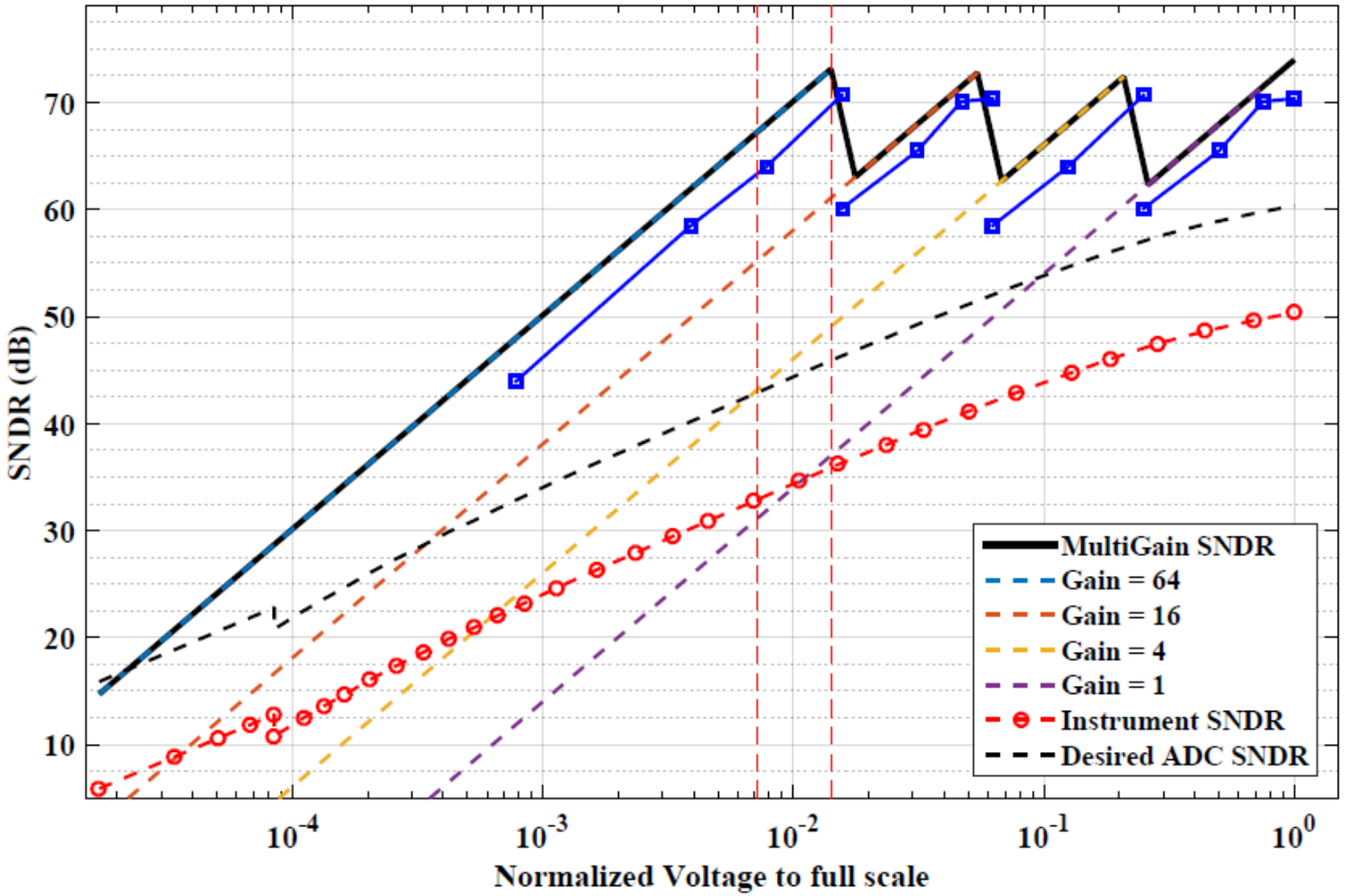
- Vin = 400mV,
- Manselect enabled
- Branch 1x selected

Sim Results@ 5MHz Input, 40MSPS

- 1.6V_{PP} differential input provided, 1x gain selected manually.
  - Similar results obtained for using 4x gain at maximum value.
- Simulations contain:
  - Transistor level transient simulation
  - Transient noise enabled
  - Input resistance of 10Ω. Bond wires not added yet.
- Tt, ff, ss, sf and fs corners simulated for 0^{o}C and 50^{o}C
  - All results better than 68.7dB SNDR
  - **Bias currents not adjusted yet** to equalize power consumption.

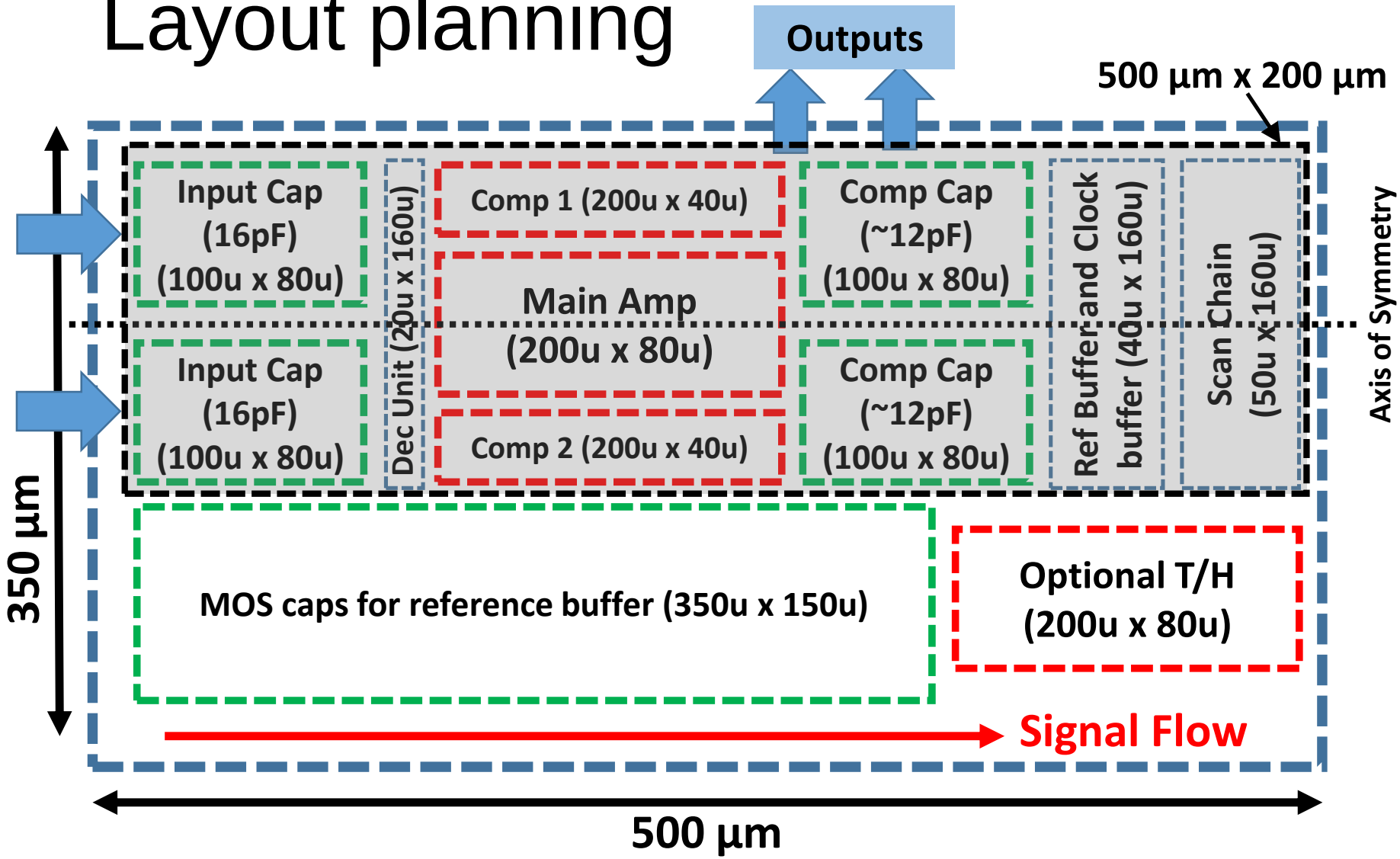
Corner	SNR (dB)	SNDR (dB)	Current (mA)	$Vout_{pp}$ (diff) (V)
tt 0	73.1	70.58	13.83	1.6
tt 50	72.38	68.7	14.6	1.6
ss0	72.33	70.7	11.96	1.6
ff 50	71.77	69.27	20.16	1.6

Current Status: With ManSel: ss0



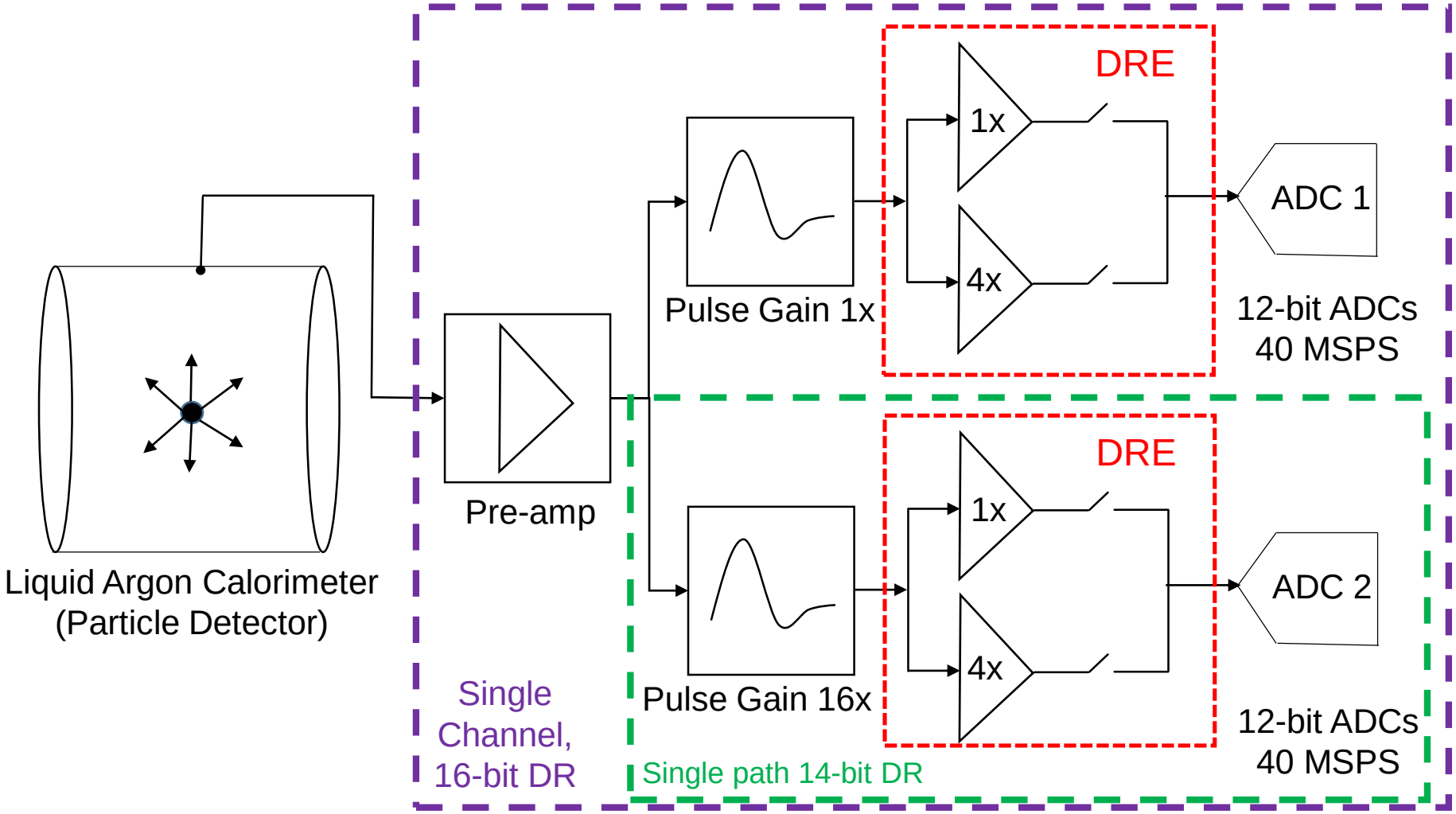
- Manual select means either one of 1x gain or 4x gain is selected for the complete experiment .

Layout planning

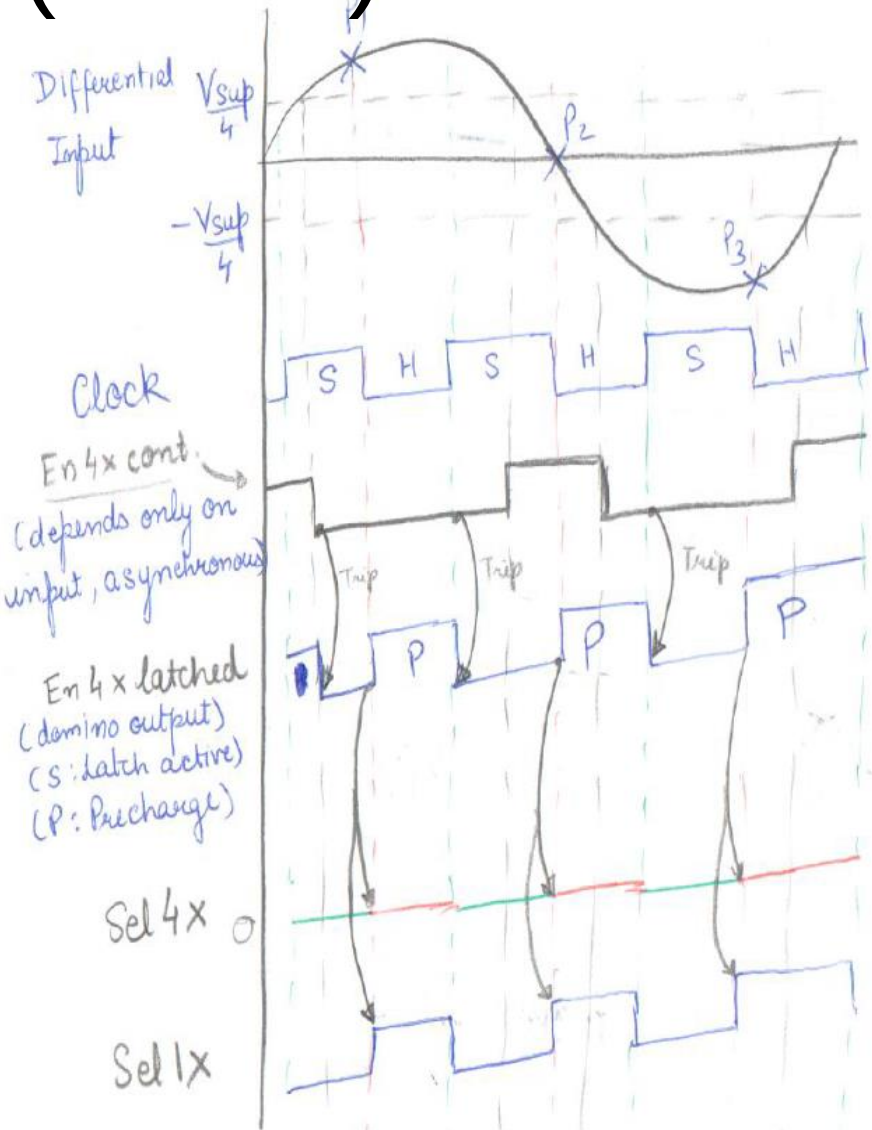


Channel area: 500 µm x 200 µm, Active area: 500 µm x 350 µm

Dual gain as DRE



Switching selection scheme (contd.)



Timing

→ S ⇒ 1x & 4x Sample

→ Hadv ⇒ Decide 1x or 4x

→ H ⇒ Either Sel 1x or Sel 4x becomes 1.

Selection process:

→ H ⇒ Precharge (P) En4x latched node (output of domino latch)

→ S ⇒ Latch active, anytime En4x cont is 0 (zero), domino trips, output 0.

→ H adv ⇒ Transfer latch value to make either sel 1x active or Sel 4x active

→ H ⇒ cycle repeats

→ During S, sel 1x & sel 4x are 0 (zero)

Switching selection scheme (contd.)